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Relevance scale

1 Design and Implementation of High-Performance Memory Systems for Future Packet Buffers

Jorge García, Jesús Corbal, Llorenç Cerdà, Mateo Valero

December 2003 **Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture**

Full text available: pdf(348.55 KB) Publisher Site

Additional Information: full citation, abstract

In this paper we address the design of a future high-speedrouter that supports line rates as high as OC-3072 (160 Gb/s),around one hundred ports and several service classes. Buildingsuch a high-speed router would raise many technological problems,one of them being the packet buffer design, mainly becausein router design it is important to provide worst-case bandwidthguarantees and not just average-case optimizations.A previous packet buffer design provides worst-case bandwidthguarantees by using ...

2 Embedded applications: Encryption overhead in embedded systems and sensor network nodes: modeling and analysis

Ramnath Venugopalan, Prasanth Ganesan, Pushkin Peddabachagari, Alexander Dean, Frank Mueller, Mihail Sichitiu

October 2003 **Proceedings of the international conference on Compilers, architectures and synthesis for embedded systems**

Full text available: pdf(293.59 KB) Additional Information: full citation, abstract, references, index terms

Recent research in sensor networks has raised issues of security for small embedded devices. Security concerns are motivated by the deployment of a large number of sensory devices in the field. Limitations in processing power, battery life, communication bandwidth and memory constrain the applicability of existing cryptography standards for small embedded devices. A mismatch between wide arithmetic for security (32 bit word operations) and embedded data bus widths (often only 8 or 16 bits) combi ...

Keywords: embedded systems, encryption, security, sensor networks

3 Architectural design for embedded systems: VL-CDRAM: variable line sized cached DRAMs

Ananth Hegde, N. Vijaykrishnan, Mahmut Kandemir, Mary Jane Irwin

October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign & system synthesis**

Full text available: pdf(382.89 KB) Additional Information: full citation, abstract, references, index terms

Many of the current memory architectures embed a SRAM cache within the DRAM memory. These architectures exploit a wide internal data bus to transfer an entire DRAM row to the on-memory cache. However, applications exhibit a varying spatial locality across the different DRAM rows that are accessed and buffering the entire row may be wasteful. In order to adapt to the changing spatial locality, we propose a Variable Line size Cached DRAM (VL-CDRAM) that can buffer portions of an accessed DRAM row. ...

Keywords: CDRAM, VL-CDRAM, energy, variable line

4 Security: Analyzing and modeling encryption overhead for sensor network nodes

Prasanth Ganesan, Ramnath Venugopalan, Pushkin Peddabachagari, Alexander Dean, Frank Mueller, Mihail Sichitiu

September 2003 **Proceedings of the 2nd ACM international conference on Wireless sensor networks and applications**

Full text available: pdf(254.57 KB) Additional Information: full citation, abstract, references, index terms

Recent research in sensor networks has raised security issues for small embedded devices. Security concerns are motivated by the deployment of a large number of sensory devices in the field. Limitations in processing power, battery life, communication bandwidth and memory constrain the applicability of existing cryptography standards for small embedded devices. A mismatch between wide arithmetic for security (32 bit word operations) and embedded data bus widths (often only 8 or 16 bits) combined ...

Keywords: analysis, embedded systems, encryption overhead, model, sensor networks

5 System level issues: Energy-aware memory allocation in heterogeneous non-volatile memory systems

Hyung Gyu Lee, Naehyuck Chang

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(59.50 KB) Additional Information: full citation, abstract, references, index terms

Memory systems consume a significant portion of power in hand-held embedded systems. So far, low-power memory techniques have addressed the power consumption when the system is turned on. In this paper, we consider data retention energy during the power-off period. For this purpose, we first characterize the data retention energy and cycle-accurate active mode energy of the non-volatile memory systems. Next, we present energy-aware memory allocation for a given task set taking into account arriv ...

Keywords: low-power memory, memory allocation, non-volatile memory

6 Effects of clock resolution on the scheduling of interactive and soft real-time processes

Yoav Etsion, Dan Tsafrir, Dror G. Feitelson

June 2003 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2003 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 31 Issue 1

Full text available: pdf(512.91 KB) Additional Information: full citation, abstract, references, index terms

It is commonly agreed that scheduling mechanisms in general purpose operating systems do not provide adequate support for modern interactive applications, notably multimedia applications. The common solution to this problem is to devise specialized scheduling mechanisms that take the specific needs of such applications into account. A much simpler

alternative is to better tune existing systems. In particular, we show that conventional scheduling algorithms typically only have little and possibly ...

Keywords: Linux, clock interrupt rate, interactive process, overhead, scheduling, soft real-time, tuning

7 MEDEA workshop: Fine-grain design space exploration for a cartographic SoC multiprocessor

Alessio Bechini, Pierfrancesco Foglia, Cosimo Antonio Prete
March 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 1

Full text available: pdf(948.91 KB) Additional Information: full citation, abstract, references, index terms

Traditionally, in the field of embedded systems low power consumption and low cost have been always regarded as stringent specification constraints. In recent years, high computational power has become a fundamental requirement as well. This has been mainly determined by the introduction of new features, typical of general-purpose systems, e.g. GUI-based interfaces. In this setting, low cost, low power consumption, significant computational power and short time-to-market are conflicting needs th ...

Keywords: SoC Multiprocessors, embedded systems, multiprocessor architecture, performance evaluation, trace-driven simulation

8 Low-energy off-chip SDRAM memory systems for embedded applications

Hojun Shim, Yongsoo Joo, Yongseok Choi, Hyung Gyu Lee, Naehyuck Chang
February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Full text available: pdf(3.98 MB) Additional Information: full citation, abstract, references, index terms

Memory systems are dominant energy consumers, and thus many energy reduction techniques for memory buses and devices have been proposed. For practical energy reduction practices, we have to take into account the interaction between a processor and cache memories together with application programs. Furthermore, energy characterization of memory systems must be accurate enough to justify various techniques. In this article, we build an in-house energy simulator for memory systems that is accelerat ...

Keywords: Low power, SDRAM, memory system

9 Measuring thin-client performance using slow-motion benchmarking

Jason Nieh, S. Jae Yang, Naomi Novik
February 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 1

Full text available: pdf(871.62 KB) Additional Information: full citation, abstract, references, citings, index terms

Modern thin-client systems are designed to provide the same graphical interfaces and applications available on traditional desktop computers while centralizing administration and allowing more efficient use of computing resources. Despite the rapidly increasing popularity of these client-server systems, there are few reliable analyses of their performance. Industry standard benchmark techniques commonly used for measuring desktop system performance are ill-suited for measuring the performance of ...

Keywords: Thin-client computing, client-server, measurement methodology, multimedia

10

The A to Z of SoCs

Reinaldo A. Bergamaschi, John Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(209.48 KB) Additional Information: full citation, abstract, references, citings, index terms

The exploding complexity of new chips and the ever decreasing time-to-market window are forcing fundamental changes in the way systems are designed. The advent of Systems-on-Chip (SoC) based on pre-designed intellectual-property (IP) cores has become an absolute necessity for embedded systems companies to remain competitive. Designing an SoC, however, is extremely complex, as it encompasses a range of difficult problems in hardware and software design. This paper explains a wide range of SoC iss ...

11 Session 7: embedded system techniques (2): Low Power Control Techniques For TFT LCD Displays

Franco Gatti, Andrea Acquaviva, Luca Benini, Bruno Ricco'

October 2002 **Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems**

Full text available: pdf(314.45 KB) Additional Information: full citation, abstract, references, citings

Display power consumption is often the most significant contributor to the overall power budget for many portable devices. Traditionally, liquid crystal display (LCD) power minimization has focused on technology and circuit design. In this paper we take an orthogonal approach, and we introduce several software-only techniques for LCD dynamic power management, which do not require any hardware changes on existing LCDs and their controllers. The power savings achieved are significant: from 40% (wi ...

12 Processor-based system: Unifying memory and processor wrapper architecture in multiprocessor SoC design

Férid Gharsalli, Damien Lyonnard, Samy Meftali, Frédéric Rousseau, Ahmed A. Jerraya

October 2002 **Proceedings of the 15th international symposium on System Synthesis**

Full text available: pdf(682.89 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a new methodology for application specific multiprocessor system-on-chip design. This approach facilitates the integration of existing components with the concept of wrapper. Wrappers allow automatic adaptation of physical interfaces to a communication network. We also give a generic architecture to produce these wrappers, either for processors or for other specific components such as memory IP. This approach has successfully been applied on a low-level image processing ...

Keywords: embedded memory, memory access, memory wrapper generation, system-on-chip

13 Lightweight network support for scalable end-to-end services

Kenneth L. Calvert, James Griffioen, Su Wen

August 2002 **ACM SIGCOMM Computer Communication Review , Proceedings of the 2002 conference on Applications, technologies, architectures, and protocols for computer communications**, Volume 31 Issue 4

Full text available: pdf(331.84 KB) Additional Information: full citation, abstract, references, citings, index terms

Some end-to-end network services benefit greatly from network support in terms of utility and scalability. However, when such support is provided through service-specific mechanisms, the proliferation of one-off solutions tend to decrease the robustness of the

network over time. Programmable routers, on the other hand, offer generic support for a variety of end-to-end services, but face a different set of challenges with respect to performance, scalability, security, and robustness. Ideally, rou ...

Keywords: end-to-end services, ephemeral state, programmable network, router achitecture

14 Session 4: Low-power color TFT LCD display for hand-held embedded systems

Inseok Choi, Hojun Shim, Naehyuck Chang

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available: pdf(690.68 KB) Additional Information: full citation, abstract, references, citings, index terms

An LCD (Liquid Crystal Display) is a standard display device for hand-held embedded systems. Today, color TFT (Thin-Film Transistor) LCDs are common even in cost-effective equipments. An LCD display system is composed of an LCD panel, a frame buffer memory, an LCD and frame buffer controller, and a backlight inverter and lamp. All of them are heavy power consumers, and their portion becomes much more dominant when running interactive applications. This is because interactive applications are oft ...

Keywords: LCD, embedded system, low energy, low power

15 Low-voltage memories for power-aware systems

Kiyoo Itoh

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available: pdf(281.56 KB) Additional Information: full citation, abstract, references, citings

This paper describes low-voltage RAM designs for stand-alone and embedded memories in terms of signal-to-noise-ratio designs of RAM cells and subthreshold-current reduction.First, structures and areas of current DRAM and SRAM cells are discussed. Next, low-voltage peripheral circuits that have been proposed so far are reviewed with focus on subthreshold-current reduction, speed variation, on-chip voltage conversion, and testing.Finally, based on the above discussion, a perspective is given with ...

Keywords: DRAM and SRAM cells, gain cells, gate-source/substrate-source back-biasing, memory-rich architectures, multi-*Vr*, non-volatile RAMs, on-chip voltage converters, peripheral circuits, subthreshold current, testing

16 Architecture: The architecture of the DIVA processing-in-memory chip

Jeff Draper, Jacqueline Chame, Mary Hall, Craig Steele, Tim Barrett, Jeff LaCoss, John Granacki, Jaewook Shin, Chun Chen, Chang Woo Kang, Ihn Kim, Gokhan Daglikoca

June 2002 **Proceedings of the 16th international conference on Supercomputing**

Full text available: pdf(295.98 KB) Additional Information: full citation, abstract, citings, index terms

The DIVA (Data IntensiVe Architecture) system incorporates a collection of Processing-In-Memory (PIM) chips as smart-memory co-processors to a conventional microprocessor. We have recently fabricated prototype DIVA PIMs. These chips represent the first smart-memory devices designed to support virtual addressing and capable of executing multiple threads of control. In this paper, we describe the prototype PIM architecture. We emphasize three unique features of DIVA PIMs, namely, the memory interf ...

Keywords: architecture, memory bandwidth, processing-in-memory

17 System on chip design: Automatic generation of embedded memory wrapper for multiprocessor SoC

Ferid Gharsalli, Samy Meftali, Frédéric Rousseau, Ahmed A. Jerraya
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(246.75 KB) Additional Information: full citation, abstract, references, citings, index terms

Embedded memory plays a critical role to improve performances of systems-on-chip (SoC). In this paper, we present a new methodology for embedded memory design in the case of application specific multiprocessor system-on-chip. This approach facilitates the integration of standard memory components. The concept of memory wrapper allows automatic adaptation of physical memory interfaces to a communication network that may have a different number of access ports. We give also a generic architecture ...

Keywords: dystem-on-chip, embedded memory, memory access, memory wrapper generation

18 Design space exploration for embedded systems: Energy exploration and reduction of SDRAM memory systems

Yongsoo Joo, Yongseok Choi, Hojun Shim, Hyung Gyu Lee, Kwanho Kim, Naehyuck Chang
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(196.08 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we introduce a precise energy characterization of SDRAM main memory systems and explore the amount of energy associated with design parameters, leading to energy reduction techniques that we are able to recommend for practical use.We build an in-house energy simulator for SDRAM main memory systems based on cycle-accurate energy measurement and state-machine-based characterizations which independently characterize dynamic and static energy. We explore energy behavior of the memory ...

Keywords: SDRAM, low power, memory system

19 Wormhole IP over (connectionless) ATM

Manolis G. H. Katevenis, Iakovos Mavroidis, Georgios Sapountzis, Eva Kalyvianaki, Ioannis Mavroidis, Georgios Glykopoulos
October 2001 **IEEE/ACM Transactions on Networking (TON)**, Volume 9 Issue 5

Full text available: pdf(211.25 KB) Additional Information: full citation, abstract, references, citings, index terms

High-speed switches and routers internally operate using fixed-size cells or segments; variable-size packets are segmented and later reassembled. Connectionless ATM was proposed to quickly carry IP packets segmented into cells (AAL5) using a number of hardware-managed ATM VCs. We show that this is analogous to wormhole routing. We modify this architecture to make it applicable to existing ATM equipment: we propose a low-cost, single-input, single-output Wormhole IP Router that functions as a VP/ ...

Keywords: Connectionless ATM, IP over ATM, gigabit router, routing filter, wormhole IP, wormhole routing

20 A dynamic-SDRAM-mode-control scheme for low-power systems with a 32-bit RISC

CPU
Seiji Miura, Kazushige Ayukawa, Takao Watanabe
August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**
Full text available: pdf(955.52 KB) Additional Information: full citation, references, citings, index terms

Keywords: SDRAM controller, active-standby mode, standby mode

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Terms used **SDRAM refresh cycle multi parallel multiprocess** Found **36** of **134,837**

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21 Lightning-2: a high-performance display subsystem for PC clusters

Gordon Stoll, Matthew Eldridge, Dan Patterson, Art Webb, Steven Berman, Richard Levy, Chris Caywood, Milton Taveira, Stephen Hunt, Pat Hanrahan

August 2001 **Proceedings of the 28th annual conference on Computer graphics and interactive techniques**

Full text available: pdf(2.06 MB) Additional Information: full citation, abstract, references, citings, index terms

Clusters of PCs are increasingly popular as cost-effective platforms for supercomputer-class applications. Given recent performance improvements in graphics accelerators, clusters are similarly attractive for demanding graphics applications. We describe the design and implementation of Lightning-2, a display subsystem for such a cluster. The system scales in both the number of rendering nodes and the number of displays supported, and allows any pixel data generated from any node to be dynamic ...

Keywords: graphics hardware, graphics systems, parallel computing, rendering hardware, rendering systems

22 Internet nuggets

Mark Thorson

June 2001 **ACM SIGARCH Computer Architecture News**, Volume 29 Issue 3

Full text available: pdf(384.73 KB) Additional Information: full citation, abstract, index terms

This column consists of selected traffic from the comp.arch newsgroup, a forum for discussion of computer architecture on Internet---an international computer network. As always, the opinions expressed in this column are the personal views of the authors, and do not necesarily represent the institutions to which they are affiliated. Text which sets the context of a message appears in italics; this is usually text the author has quoted from earlier messages. The code-like expressions below the au ...

23 Optimizing software performance for IP frame reassembly in an integrated architecture

Peter M. Ewert, Naraig Manjikian

September 2000 **Proceedings of the second international workshop on Software and performance**

Full text available: pdf(132.48 KB) Additional Information: full citation, references, index terms

Keywords: asynchronous transfer mode, communication processors, computer architecture, event-driven simulation, software performance

24 Polygon rendering on a stream architecture

John D. Owens, William J. Dally, Ujval J. Kapasi, Scott Rixner, Peter Mattson, Ben Mowery

August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(161.65 KB) Additional Information: full citation, abstract, references, citings, index terms

The use of a programmable stream architecture in polygon rendering provides a powerful mechanism to address the high performance needs of today's complex scenes as well as the need for flexibility and programmability in the polygon rendering pipeline. We describe how a polygon rendering pipeline maps into data streams and kernels that operate on streams, and how this mapping is used to implement the polgyon rendering pipeline on Imagine, a programmable stream processor. We compare our resul ...

Keywords: OpenGL, SIMD, graphics hardware, kernels, media processors, polygon rendering, stream architecture, stream processing, streams

25 A programmable built-in self-test core for embedded memories

Chih-T. Huang, Jing-R. Huang, Cheng-W. Wu

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(91.92 KB) Additional Information: full citation, references

26 Array allocation taking into account SDRAM characteristics

Hong-Kai Chang, Youn-Long Lin

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(95.08 KB) Additional Information: full citation, references, citings

27 A low-cost memory architecture for PCI-based interactive ray casting

Michael Doggett, Michael Meißner, Urs Kanus

July 1999 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.12 MB) Additional Information: full citation, references, citings, index terms

Keywords: graphics hardware, memory architecture, raycasting, volume rendering accelerator, volume visualization

28 Hybrid volume and polygon rendering with cube hardware

Kevin Kreeger, Arie Kaufman

July 1999 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.85 MB) Additional Information: full citation, references, citings, index terms

Keywords: cube architecture, mixing polygons and volumes, ray casting, run-length-encoding, volume rendering

29 A performance comparison of contemporary DRAM architectures
Vinodh Cuppu, Bruce Jacob, Brian Davis, Trevor Mudge
May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2
Full text available: pdf(166.88 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In response to the growing gap between memory access time and processor speed, DRAM manufacturers have created several new DRAM architectures. This paper presents a simulation-based performance study of a representative group, each evaluated in a small system organization. These small-system organizations correspond to workstation-class computers and use on the order of 10 DRAM chips. The study covers Fast Page Mode, Extended Data Out, Synchronous, Enhanced Synchronous, Synchronous Link, Rambus, ...

30 Microservers: a new memory semantics for massively parallel computing
Jay B. Brockman, Peter M. Kogge, Thomas L. Sterling, Vincent W. Freeh, Shannon K. Kuntz
May 1999 **Proceedings of the 13th international conference on Supercomputing**
Full text available: pdf(1.40 MB) Additional Information: full citation, references, citings, index terms

Keywords: massively parallel, microserver, processing-in-memory

31 A parallel embedded-processor architecture for ATM reassembly
Richard F. Hobson, P. S. Wong
February 1999 **IEEE/ACM Transactions on Networking (TON)**, Volume 7 Issue 1
Full text available: pdf(331.21 KB) Additional Information: full citation, references, citings, index terms

Keywords: ATM, embedded systems, medium access control, segmentation and reassembly

32 Neon: a single-chip 3D workstation graphics accelerator
Joel McCormack, Robert McNamara, Christopher Gianos, Larry Seiler, Norman P. Jouppi, Ken Correll
August 1998 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Full text available: pdf(1.58 MB) Additional Information: full citation, references, citings, index terms

Keywords: chunk rendering, direct rendering, graphics pipeline, level of detail, rasterization, texture cache, tile rendering

33 EM-Cube: an architecture for low-cost real-time volume rendering
Rändy Osborne, Hanspeter Pfister, Hugh Lauer, TakaHide Ohkami, Neil McKenzie, Sarah Gibson, Wally Hiatt

August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Full text available: pdf(1.04 MB) Additional Information: full citation, references, citings, index terms

34 Missing the memory wall: the case for processor/memory integration
Ashley Saulsbury, Fong Pong, Andreas Nowatzyk
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2
Full text available: pdf(1.45 MB) Additional Information: full citation, abstract, references, citings, index terms

Current high performance computer systems use complex, large superscalar CPUs that interface to the main memory through a hierarchy of caches and interconnect systems. These CPU-centric designs invest a lot of power and chip area to bridge the widening gap between CPU and main memory speeds. Yet, many large applications do not operate well on these systems and are limited by the memory subsystem performance.This paper argues for an integrated system approach that uses less-powerful CPUs that are ...

35 Dynamic scheduling and synchronization synthesis of concurrent digital systems under system-level constraints
Claudionor N. Coelho, Giovanni De Micheli
November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(783.93 KB) Additional Information: full citation, abstract, references, citings, index terms

We present in this paper a novel control synthesis technique for system-level specifications that are better described as a set of concurrent synchronous descriptions, their synchronizations and constraints. The proposed synthesis technique considers the degrees of freedom introduced by the concurrent models and by the environment in order to satisfy the design constraints.Synthesis is divided in two phases. In the first phase, the original specification is translated into an alg ...

36 FBRAM: a new form of memory optimized for 3D graphics
Michael F. Deering, Stephen A. Schlapp, Michael G. Lavelle
July 1994 **Proceedings of the 21st annual conference on Computer graphics and interactive techniques**
Full text available: pdf(67.48 KB) ps(157.07 KB) Additional Information: full citation, abstract, references, citings, index terms

FBRAM, a new form of dynamic random access memory that greatly accelerates the rendering of Z-buffered primitives, is presented. Two key concepts make this acceleration possible. The first is to convert the read-modify-write Z-buffer compare and RGB&agr; blend into a single write only operation. The second is to support two levels of rectangularly shaped pixel caches internal to the memory chip. The result is a 10 megabit part that, for 3D graphics, performs read-modify-write cycles ten tim ...

Keywords: 3D graphics hardware, caching, dynamic memory, parallel graphics algorithms, rendering